

**REPLY UNDER 37 C.F.R. §1.116  
EXPEDITED PROCEDURE  
TECHNOLOGY CENTER ART UNIT 2826**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of

YONEMARU Atty. Ref.: 829-618; Confirmation No. 3114

Appl. No. 10/720,764 TC/A.U. 2826

Filed: November 25, 2003 Examiner: DICKEY, T.

For: SEMICONDUCTOR INTEGRATED LOGIC CIRCUIT INCLUDING TWO PMOS  
TRANSISTORS CONNECTED IN SERIES AND TWO NMOS TRANSISTORS  
CONNECTED IN SERIES

\* \* \* \* \*

July 7, 2008

Mail Stop AF  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

**AMENDMENT AFTER FINAL REJECTION**

Responsive to the Official Action dated April 8, 2008, please amend the above-identified  
application as follows:

**DO NOT ENTER  
TD 7/18/08**